ANALYTICAL CHARGE CONSERVATIVE LARGE SIGNAL MODEL FOR MODFETS VALIDATED UP TO MM-WAVE RANGE

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ABSTRACT

We present an analytical charge conservative large signal model for MODFETs, which is valid up to mm-wave frequencies. Although the model equations are simple, an excellent accuracy in the representation of the nonlinear elements of the FET is achieved. The model was used for the successful design of a 2-stage power amplifier for 60 GHz.

INTRODUCTION

There is an urgent need for accurate large signal models for MODFETs which can be used for computer aided design of monolithic integrated nonlinear circuits operating up to the millimeter-wave range. For large signal models it is important to include charge conservation to improve the model consistency and the convergence properties of the nonlinear simulation [1], [2], [3]. We introduce in this contribution an analytical large signal model for MODFETs which is charge conservative and contains simple equations to represent the voltage dependent elements of the FET very accurately. The model parameters were extracted for a PM-MODFET (l_g=0.15 µm, w_g=120 µm) and verified with both small signal and large signal measurements at different bias conditions. By performing these measurements for devices with different gate widths, the scaling properties of the model were verified. The model was successfully used in the design of a 2-stage power amplifier for 60-GHz achieving the predicted performance of P_{sat} = 23 dB (at 2.5 dB gain compression) and 10 dB small signal gain in the first design cycle.

LARGE SIGNAL MODEL

In Fig. 1 the equivalent circuit of the large signal model is depicted. The intrinsic part is enclosed by the dashed line. The current generators I_{ds}, I_{gs}, I_{gd} and the bias dependent capacitances C_{gs} and C_{gd} are considered as the nonlinear elements in the model.
Bias dependent S-parameters and dc-measurements from a PM-MODFET (l_g=0.15 µm, w_g=120 µm) were used for the extraction of the model parameters. The intrinsic elements were calculated after de-embedding of the parasitics from measured S-parameters.
For the I_{gs} and I_{gd} current generators the diode equation for both, the forward and reverse bias mode was used. Equation (1) with the forward bias fitting parameters I_{ss} and n represents the diode current for positive diode voltage.

$$I_{diode}\left(V_{diode}\right) = I_{ss}\left(e^{\frac{V_{diode}}{n \cdot Vt}} - 1\right) \qquad (1)$$

Forward and reverse bias mode parameters were extracted from the gate current measured at zero drain bias. Fig. 2 shows the simulated and measured diode current after parameter extraction.
The drain-source current generator I_{ds} is represented by the nonlinear equation (2), [4]. The equation consists of 10 parameters, which are fitted to the DC-IV-output characteristic, considering also g_m and g_{ds} calculated from S-parameters.

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$$I_{ds}\left(V_{gsi}, V_{dsi}\right) = f_1\left(V_{gsi}\right)\cdot\left(1+\frac{\lambda}{1+\Delta_\lambda\cdot\left(V_{gsi}-V_{to}\right)^2}\cdot V_{dsi}\right)\cdot\tanh\left(\alpha\cdot V_{dsi}\right)$$

$$f_1\left(V_{gsi}\right) = CD_{vc}\cdot\left(1+\tanh\left[\beta\cdot\left(V_{gsi}-V_c\right)+\gamma\cdot\left(V_{gsi}-V_c\right)^3\right]\right)+CD_{vsb}\cdot\left(1+\tanh\left[\delta\cdot\left(V_{gsi}-V_{sb}\right)\right]\right) \qquad (2)$$

$$V_{to} = V_c - \frac{2}{\beta}$$

Fig. 3 shows the comparison of the measured with simulated data after this extraction step

In order to consider charge conservation and to model the nonlinear capacitances C_{gs} and C_{gd} very accurately we use equation (3) for the gate charge. Differentiating Q_g with respect to V_{gsi} and V_{dsi} leads to the input capacitance C_{11} ($=C_{gs}+C_{gd}$) and to the transcapacitance C_{12} ($=-C_{gd}$) respectively. A total of 9 parameters is fitted to the measured capacitances. The results are depicted in Fig. 4.

$$Q_g\left(V_{gsi}, V_{dsi}\right) = A\cdot\left[f_1\cdot f_2\right]+E\cdot\left[V_{gsi}-0.5\cdot V_{dsi}\right]$$

with

$$f_1 = \frac{1}{B}\cdot\ln\left[\cosh(B\cdot w)\right]+w \qquad (3)$$

$$w = \left(V_{gsi}-V_1\right)-0.5\cdot\tanh\left(C\cdot V_{dsi}\right)$$

$$f_2 = D\cdot\ln\left[\cosh\left(F\cdot V_{dsi}\right)\right]+1$$

VERIFICATION

The model was implemented as a user defined model in the MDS simulator (HP-EEsof). The equivalent circuit in Fig. 1 enforces that the gate charge has to be divided into two respective portions. Partition was performed by the equations (4) proposed in [5], where the parameters CGDSAT and DELTDS are also discussed.

After the extraction of the model parameters was completely performed, simulated S-parameters at different bias points were compared with measured data. Fig. 5 shows the comparison for 4 different operating regions of the PM-MODFET. Finally, large signal measurements at a fundamental frequency of 25 GHz from devices with different gate width were compared with simulated data. In Fig. 6 the comparison is depicted. Because the impedance of the measurement system is 50 Ohm the maximal available output power is not achieved. The comparison demonstrates that the model is fully scaleable with the gate width. The model was used to design a 2-stage PM-MODFET power amplifier for an operating frequency of 60 GHz with our CPW-Library [6]. Small signal and large signal measurements of the fabricated amplifier (Fig. 7) are compared with the simulated data in Fig. 8 and Fig. 9 respectively. Predicted and achieved performance are in a very good agreement.

$$Q_{gs}\left(V_{gsi}, V_{dsi}\right) = \left[Q_g - CGDSAT\cdot\left(V_{gsi}-V_{dsi}\right)\right]\cdot g_1\left(V_{dsi}\right)+CGDSAT\cdot V_{gsi}\cdot g_2\left(V_{dsi}\right)$$

$$Q_{gd}\left(V_{gsi}, V_{dsi}\right) = \left[Q_g - CGDSAT\cdot V_{gsi}\right]\cdot g_2\left(V_{dsi}\right)+CGDSAT\cdot\left(V_{gsi}-V_{dsi}\right)\cdot g_1\left(V_{dsi}\right) \qquad (4)$$

with $g_1\left(V_{dsi}\right) = 0.5\cdot\left[1+\tanh\left(\frac{3}{DELTDS}\cdot V_{dsi}\right)\right]$

$$g_2\left(V_{dsi}\right) = 0.5\cdot\left[1-\tanh\left(\frac{3}{DELTDS}\cdot V_{dsi}\right)\right]$$

CONCLUSION

A large signal model was introduced, which considers charge conservation in the equation for the nonlinear capacitances. Although the model equations are relatively simple, they are capable to represent the bias dependency of the nonlinear elements very accurately. Small and large signal measurements at different bias voltages and for devices with different gate width was used for the verification of the extracted model. A 2-stage PM-MODFET power

amplifier for 60 GHz with P_{sat} = 23 dB (at 2.5 dBm gain compression) and 10 dB small signal gain was successful designed using the large signal model.

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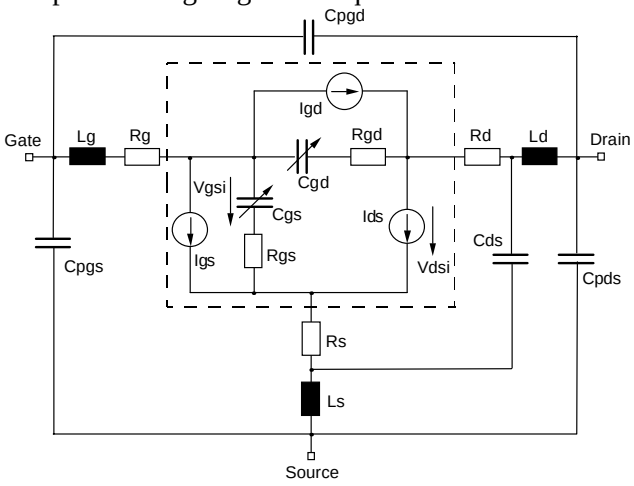

Fig. 1 Equivalent circuit for the FET.

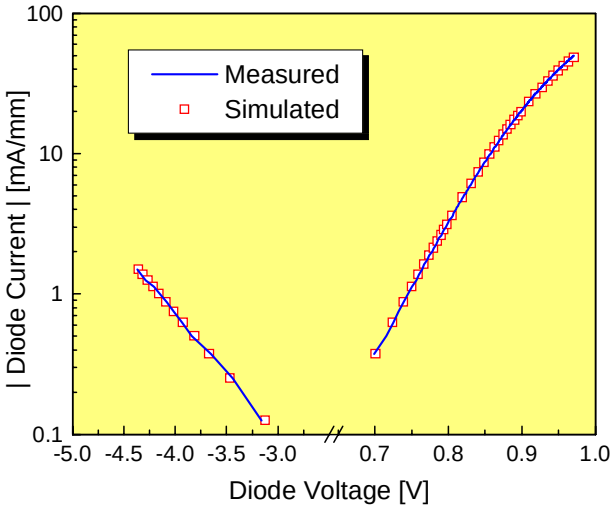

Fig. 2 Results of parameter extraction for the diode equation.

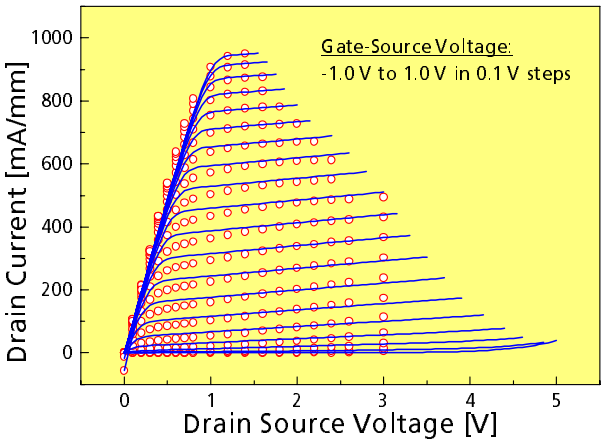

Fig. 3 Comparison of the simulated (line) and measured (circles) IV-curves.

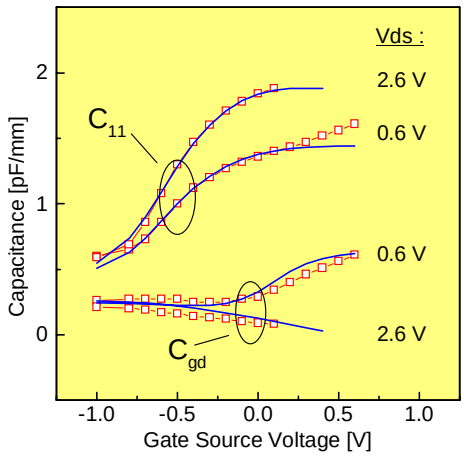

Fig. 4 The measured (squares) bias dependent capacitances are compared with simulated data (solid line) resulting in good agreement.

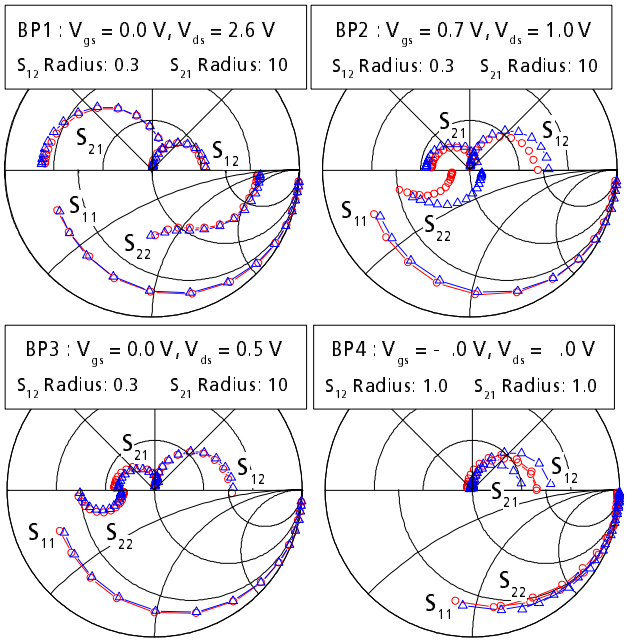

Fig. 5 Comparison of the model (circle) with measured (triangle) S-parameters (0.5 to 48 GHz) for different operating regions of the MODFET with w_g=120 µm.

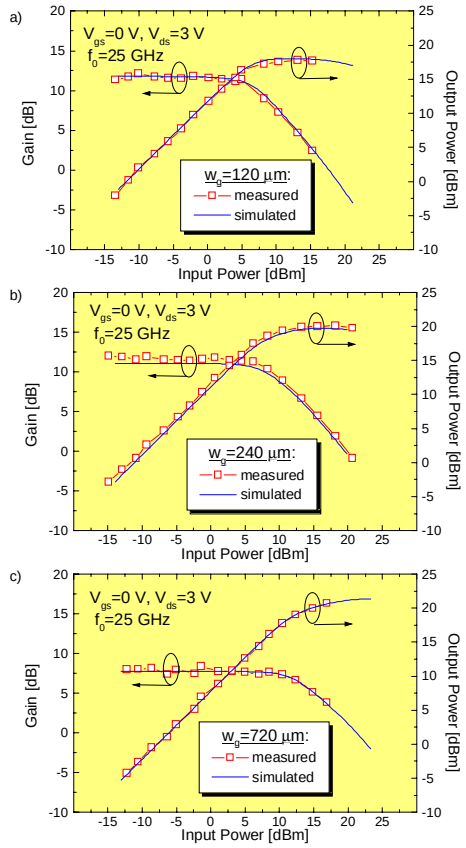

Fig. 6 Comparison with measured large signal data of MODFETs with different gate widthw_g.

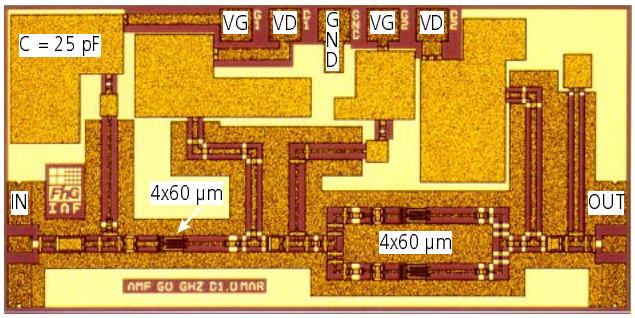

Fig. 7 Photograph of the 2-stage amplifier (1x2 mm^2) for 60 GHz using PM-MODFETs.

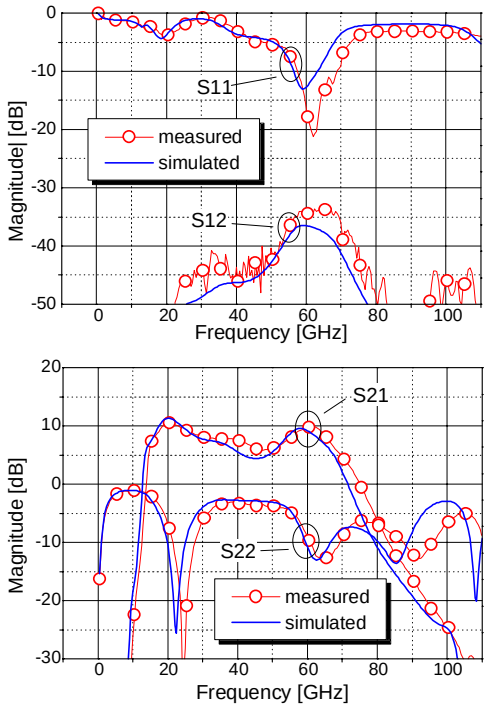

Fig. 8 Measured and simulated S-parameters of the 60 GHz amplifier. V_{gs}=0 V, V_{ds}=3.0 V.

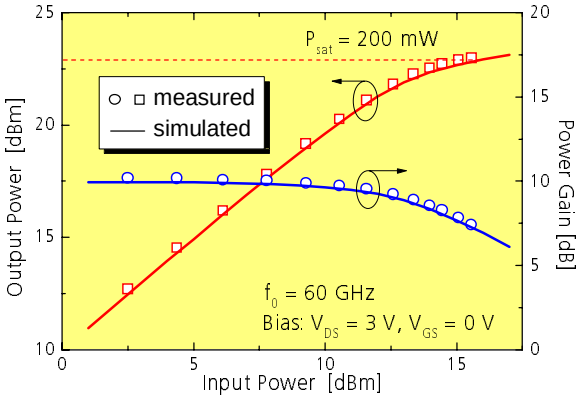

Fig. 9 Measured and simulated large signal data of the 60 GHz amplifier: G_o=10 dB, P_{-1dB}=21.8 dBm, P_{sat}=23 dBm (2.5 dB gain compression).